A Dual-band Tri-mode CDMA IF Receiver with Programmable Channel-Match Filter

Joshua Cho, Pete Good, Manish Kamat, Evan McCarthy, Keith Rampmeier*, Wim Cops**, Abdellatif El Moznine**, Hiep Truong, Yong He, Dave Yates, Georgi Taskov, Chang-hyeon Lee, Dongsoo Koh, and Stephen Lloyd
Skyworks Solutions Inc, Irvine, CA 92612 U.S.A.
** RF Magic, Inc., San Diego, CA 92121 U.S.A.*
***Conexant Systems, Newport Beach, CA 92660 U.S.A.*
Joshua.cho@skyworksinc.com

Abstract

An integrated dual-band tri-mode CDMA IF Receiver with programmable channel-match filter is presented. The cascaded VGA and filter chain provides maximum voltage gain of 93dB with noise figure of <7.5dB. It also provides >88dB of gain control range. The IF VCO, which operates at 2xLO for PCS mode and 4xLO for AMPS/CDMA mode, achieves −131dBc/Hz of phase noise at 900KHz offset with an external tank. An area-efficient combined channel-match filter chain for both CDMA/PCS and AMPS mode is realized by changing the clock frequency of a switched-capacitor filter and by switching-in and -out capacitors for the continuous time and switch-cap filters depending on the mode of operation. The filter chain meets all the blocker requirements for both CDMA/PCS and AMPS modes. Combining CDMA/PCS and AMPS filter saves 30% die area compared to separate filter chains. The IC is fabricated in Jazz's 35GHz ft Silicon BiCMOS process and packaged into a 48-pin 6mm x 6mm land grid array (RF-LGA™) chipscale package.

1. Introduction

Obtaining a programmable IF/mixed-signal circuit to accommodate multi-mode and multi-band operations will be a stepping stone to achieve a software radio that may not be possible until we can achieve high-speed and wide dynamic range ADC (Analog-Digital Converter) [1]. To accommodate the customer's needs to build the best performing CDMA cellular systems, we needed to come up with an IF receiver with dual-band and tri-mode capability with minimum die size. In this paper, a dual-band tri-mode IF receiver with programmable channel-match filter is presented. We needed to have the programmable filter to accommodate two modes of operation with one filter chain in a minimum die size. The chip with combined filter occupied 30% less die area compared to the one with two separate filter chains.

2. Architecture

The simplified block diagram of the device is shown in Fig.1.

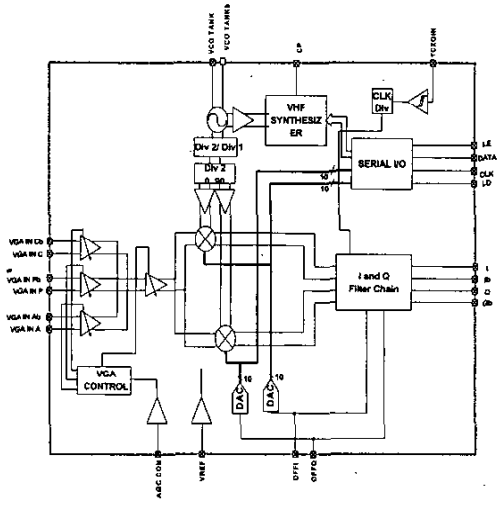

Figure 1. IC block diagram

The VGA section receives the down-converted signal from the mixer in a RF front-end IC and amplifies the signal depending on the VGA control voltage. There are three VGA inputs to accommodate the three modes of operation; i.e., AMPS, CDMA, and PCS modes. The amplified signal then goes through the I and Q quadrature mixers and is mixed down to base-band frequency. The quadrature IF LO signals are generated by the on-chip VCO and divider. The synthesizer together with the TXCO buffer provides the necessary channel programming capability using a reference signal from an external TCXO. The down-converted base-band signal is then passed through the channel-match filter chain before subsequent signal processing.

0-7803-7694-3/03/$17.00 © 2003 IEEE

3. Circuit Design for Non-filter Section

3.1 VGA and I/Q Demodulator

The Variable Gain Amplifier (VGA) has about 93dB of voltage gain and more than 88dB of gain control range [2]. This gain control range meets the required specification for CDMA systems. The VGA consists of two gain amplifiers with the contribution of each amplifier varied depending on the control voltage. The high-gain amplifier provides the maximum gain needed and the low-gain amplifier achieves the necessary linearity at low gain mode. A near-linear voltage to current conversion and then current to gain conversion are implemented.

Fully differential input stages for all three modes of operation (AMPS, CDMA, and PCS) are used to avoid any asymmetric coupling of LO signal into VGA that will be self-mixed with the LO and then generate DC offset.

The amplified signal then goes through the I and Q demodulators to generate the base-band signal.

3.2 VCO and Synthesizer

A 350MHz differential VCO with external tank is implemented. It has an amplitude-leveling loop to control the output amplitude for better phase noise and quadrature generation independent of tank Q variation [3]. The quadrature LO is generated by a divide-by-2 circuit to save area that may be required for a RC polyphase circuit at IF frequency.

The synthesizer consists of an 8/9 prescaler and a programmable integer-N divider. A programmable reference divider is also implemented.

4. Circuit Design for Filter Chain

4.1 Filter Architecture

Switched-capacitor filter (SCF) is chosen because no tuning algorithm or trimming is necessary to deal with performance variations with process. Switch-cap filter is also a preferred choice for programmability since we can easily adjust the filter cut-off frequency by varying the clock frequency.

The filter chain block diagram is shown in Fig. 2. The anti-aliasing filter consists of a 5th-order continuous-time Chebyshev filter (CTF1). The switch-cap filter consists of a 5th-order Elliptic filter and has three stages. The first stage is the sample-hold stage that also works as a low pass filter. The second and third stages are biquads. Then a 5th-order continuous-time Chebyshev filter (CTF2) follows as a recontruction filter before the signal goes out to a base-band IC.

Table 1 shows the differences in filter specification between CDMA/PCS and AMPS mode.

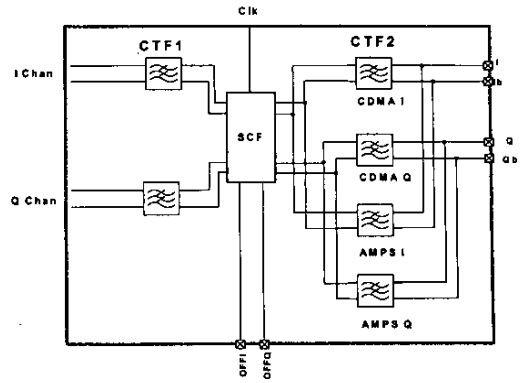

Figure 2. Block diagram for combined filter chain

Table 1. Comparison of filter specs for CDMA/PCS and AMPS modes

Item	CDMA/PCS	AMPS
Filter Bandwidth	630KHz	21KHz
Input referred noise (integrated across BW)	-80dBv	-78dBv
Group Delay variation, in-band	2.8uS	17uS
In-band ripple	+/-0.75dB	+/-0.5dB
Attenuation(CDMA/PCS) 900KHz >1.2MHz	 48dB 50dB	
Attenuation (AMPS) 21KHz 30KHz 45KHz >60KHz		 3dB 35dB 60dB 60dB

4.2 First Continuous Time Filter (CTF1)

As shown in Fig. 2, the CDMA/PCS and AMPS mode CTF1s have been combined into one filter for I and Q channels, respectively. Since the first CTFs have the largest capacitors due to noise requirement and the AMPS mode has smaller bandwidth, we shared the capacitors from AMPS mode to realize the continuous time filter for the CDMA/PCS mode.

4.3 Switched-Capacitor filter

The switch-cap filter uses a multiplexed OP-amp scheme to save power for I and Q channels. The basic idea of the scheme is to share the OP amps between I and Q channels at different phases of the switch-cap clocks. There are only 5 OP amps to realize the I and Q channels of the 5th order Elliptic filter.

The CDMA and PCS modes have the same filter requirements. But they have different requirements from AMPS mode as is shown in Table 1. The filter bandwidth difference between the two modes can be

dealt with by adjusting the clock frequency. By adjusting the clock frequency from 4.8MHz in CDMA/PCS mode to 150KHz in AMPS mode, we can adjust the filter bandwidth from 630KHz to 21KHz. The filter bandwidth of 21KHz is high compared to 12.5KHz of signal bandwidth in AMPS mode and may degrade the total noise obtained by integrating across the filter bandwidth. But since the total system bandwidth is 12.5KHz and should be determined by the digital filter in the base-band integrated circuit, the noise contribution from 12.5KHz to 21KHz will not degrade the total system SNR.

Another important consideration that is taken into account in determining the AMPS clock frequency is that the in-band (100Hz~12.5KHz) group delay of AMPS mode will be degraded if we reduced the clock frequency lower than 150KHz. This degradation of group delay at low clock frequency results from the fact that the group delay optimized for CDMA mode does not scale properly as the clock frequency is scaled, which is a down side of obtaining AMPS mode filter by just scaling clock frequency.

Next, the different blocker requirement for two different modes of operation has to be met. In CDMA/PCS mode, the SCF notches need to be placed at 900KHz and 1.7MHz while in AMPS mode they need to be at 60KHz and 120KHz. To place notches at different frequencies for different modes of operation, we have to change the sizes of a few capacitors inside the switched-capacitor filter. Figure 3 shows the jammer diagram for AMPS mode in which the attenuation specification for different jammers is shown. Since the switch-cap clock frequency of 150KHz for the AMPS mode does not meet the Nyquist criteria for the second jammer at 120KHz, the switched-cap circuit is optimized to give the best rejection of the aliased jammer at 30KHz (150-120KHz). The aliased blocker at 30KHz due to +17dBc blocker located at 120KHz is much less than 35dB below the signal level of –58dBv.

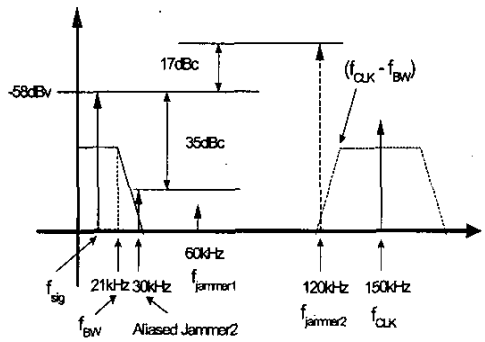

Figure 3. Jammer diagram for AMPS mode

4.4 Second Continuous Time Filter (CTF2)

Since the noise requirement for the second continuous time filter is relaxed due to large gain in SCF (>30dB), the cap sizes are smaller than those of CTF1s. Hence, the capacitor sharing scheme is not incorporated in CTF2s as shown in Fig. 2.

4.5 DC offset correction

The entire signal path from the IF input to the base-band output has about 93dB of maximum voltage gain. The LO signal can be coupled into the VGA, then be self-mixed with a large LO, and introduce some offset at the base-band output. Any mismatches in the fully differential VGA and down-conversion mixer will further increase the offset. A DC offset correction scheme is implemented assuming the base-band signal processing IC provides us with the estimation of the offset in digital form. A DAC (digital-to-analog converter) is designed to nullify the offset at the switch-cap output.

5. Test results

Measured VGA control curve versus control voltage is shown in Fig. 4. More than 88dB VGA control range is obtained.

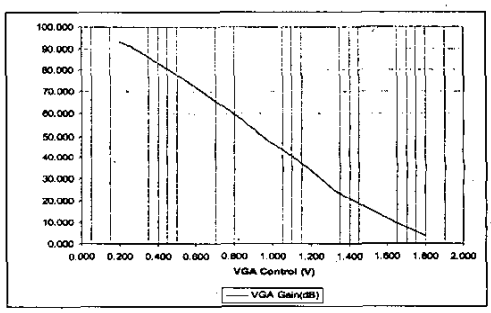

Figure 4. Measured VGA gain versus control voltage in PCS mode.

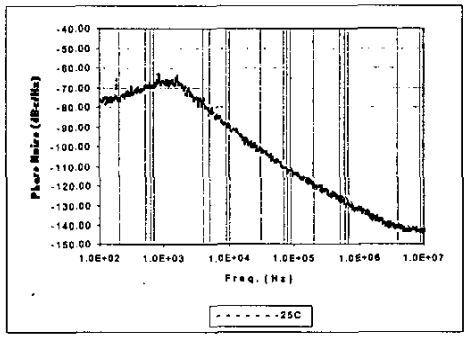

Figure 5. Measured VCO phase noise performance at 341.52MHz

Measured VCO Phase noise performance is shown in Fig. 5. Phase noise of <-70 dBc/Hz at 3KHz offset and -131dBc/Hz at 900KHz offset is obtained. It is sufficient for meeting the reciprocal mixing specification in AMPS mode.

The measured CDMA/PCS filter frequency response is shown in Fig. 6. The attenuation at 900KHz >48dB is obtained (first marker located at 300KHz).

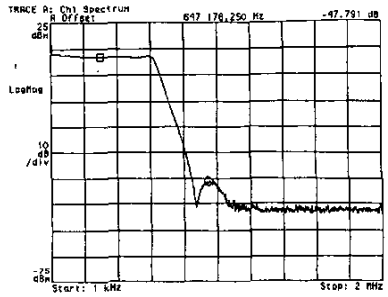

Figure 6. Measured CDMA/PCS filter response

The measured AMPS filter frequency response is shown in Fig. 7. We have >60dB attenuation of blockers at 60KHz and >40dB rejection of the 120KHz blocker aliased at 30KHz (first marker located at 10KHz).

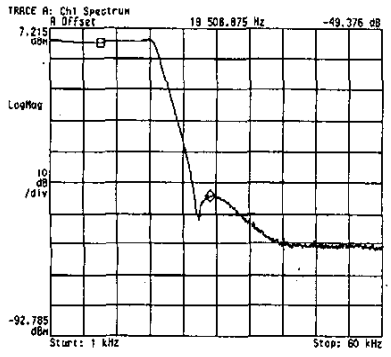

Figure 7. Measured AMPS filter response

6. Summary

A 2.7V dual-band tri-mode CDMA IF receiver with programmable channel-match filter has been presented. It meets all the noise and gain requirement of the CDMA IF section. Especially, the combined filter for both CDMA/PCS and AMPS modes meets all the filter requirements, including the different blocker specs for each mode of operation. The combined filter architecture results in a 30% die area saving compared to independent CDMA/PCS and AMPS filter chains. A summary of the measured results is presented in Table 2. The IC is packaged in a 6mm x 6mm LGA package even though it was packaged in a 7mm x 7mm LGA in a prototype build. A photomicrograph of the integrated circuit is shown in Fig.8.

Table 2. Summary of IC performance

VGA Section:	
Max Voltage Gain for VGA+Filter	93dB
Noise Figure for VGA+Filter at max gain	<7dB
IIP3 for VGA+Filter at 86dB gain	-38dBm
Filter Section:	
Filter Cut-off for CDMA/PCS	630KHz
Filter Cut-off for AMPS	21KHz
Filter Attenuation at 900KHz for CDMA/PCS	>48dB
Filter Attenuation at 60KHz for AMPS	>60dB
Filter Attenuation at 120KHz (aliased at 30KHz) for AMPS	>35dB
VCO and Synthesizer section:	
Phase noise @ 900KHz offset from 341.52MHz carrier	-131dBc/Hz
Reference Spur	<-70dBc
PLL Lock Time	<2mS

7. Acknowledgements

The authors would like to thank Tam Phan, Martin Orozco, Theresa Wisler, Frank Intveld, Marc Gougeon, Quang Nguyen, and Ron Hlavac for their support.

[1] Evening Discussion Session, "Software radio: Cool or to be Cooled," IEEE ISSCC, February 2002.
[2] K. Rampmeier, B. Agarwal, P. Mudge, D. Yates, T. Robinson, "A Versatile Receiver IC Supporting W-CDMA, CDMA, and AMPS Cellular Handset Applications," IEEE RFIC Symposium, pp., June, 2001.
[3] M. Margarit, J. Tham, R. Meyer, and M. Deen, "A low-Noise, Low-Power VCO with Automatic Amplitude Control for Wireless Applications," IEEE J. Solid-State Circuits, Vol. 34 No. 6, June 1999.

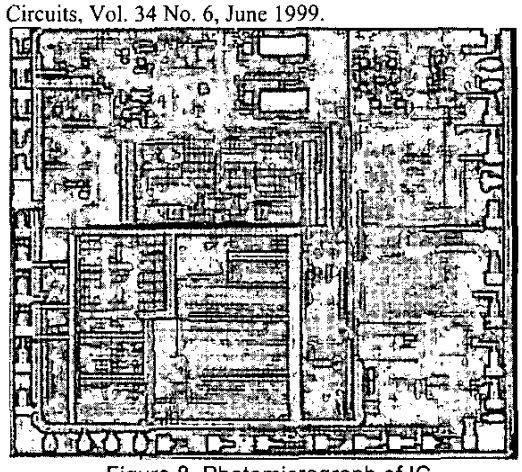

Figure 8. Photomicrograph of IC